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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/499,598	02/07/2000	Mick Henniger	4103-40821	1489

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EXAMINER
MAHMOUDI, HASSAN

ART UNIT	PAPER NUMBER
2175	6

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/499,598	Applicant(s) HENNIGER ET AL.	
	Examiner Tony Mahmoudi	Art Unit 2175	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

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Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Anderson (U.S. Patent No. 6,003,130.)

As to claim 1, Anderson teaches an apparatus (see Abstract) for use in boot-up of an electronic device (see figure 3, and see column 4, lines 44-60) which includes a motherboard and a daughterboard (see Abstract) comprising:

first data storage device, accessible to the motherboard (see figure 2), storing daughterboard boot-up code (see Abstract);

a coupler, coupling the daughterboard to the motherboard, defining at least a first data communication path from the motherboard to the daughterboard (see figures 2 and 4, and see column 3, lines 28-36);

a microprocessor positioned on the daughterboard, wherein the microprocessor includes a development port (see column3, lines 28-30, and see column 6, lines 9-26); and

at least a second communication path, defined on the daughterboard, providing for communication from the coupler to the development port (see figures 2 and 4);

wherein the boot-up code can be provided from the storage device, over the first communication path, the coupler and the second communication pathway, to the development port of the microprocessor on the daughterboard (see Abstract, figures 2 and 3, and see column 4, lines 33-43.)

As to claim 2, Anderson teaches wherein the motherboard is configured to download at least the boot-up code, to the development port automatically, in response to a power up or a reset of the electronic device (see column 4, lines 44-67, and see column 6, lines 14-26.)

As to claims 3, 6 and 14, Anderson teaches wherein the daughterboard includes a DRAM (see figure 2) and a memory controller (see figure 2) and wherein the boot-up code includes memory controller configuration information (see column 2, line 59 through column 3, line 22.)

As to claim 4, Anderson teaches a method for performing boot-up in an electronic device (see column 5, lines 13-17) including a motherboard and a coupled daughterboard (see figure 2), the daughterboard including a microprocessor having a development port (see figure 2), comprising:

automatically downloading at least first boot-up code from the motherboard to the development port, in response to a power-on or reset of the electronic device (see column 4, lines 44-67, and see column 6, lines 14-26); and

using the boot-up code, in the microprocessor of the daughterboard, for performing at least a first boot-up operation (see column 5, lines 13-17.)

As to claims 5 and 12, Anderson teaches wherein the boot-up operation includes configuring a port, different from the development port (see column 5, lines 60-63.)

As to claims 7 and 15, Anderson teaches the method further comprising downloading at least a portion of an operating system for the microprocessor, from the motherboard, using the development port (see column 1, lines 56-67.)

As to claims 8 and 16, Anderson teaches wherein the step of downloading the at least first boot-up code is performed while the daughterboard is coupled to the motherboard (see column 3, lines 23-41.)

As to claims 9 and 17, Anderson teaches wherein the step of downloading the at least first boot-up code is performed in the absence of coupling the development port to an external emulator (see column 2, lines 1-11.)

As to claims 10 and 18, Anderson teaches wherein the first boot-up operation is performed in the absence of storing the boot-up code on a daughterboard non-volatile memory prior to the power-up or reset (see column 3, lines 2-22.)

As to claim 11, the applicant is kindly directed to discussions and remarks made in claims 1 and 4 above.

As to claim 13, Anderson teaches wherein the means for performing the first boot-up operation includes means for initializing DRAM chip selects (see column 4, lines 1-3, and see lines 33-43.)

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of art with respect to methods and systems of boot-up procedures and port development for boot-up processes in general:

Patent/Pub. No.	Issued to	Cited for teaching
US 6,161,177	Anderson	Method for performing boot-up in electronic devices.
US 6,105,136	Cromer et al.	System with motherboard coupled to daughterboard.

4. Any inquiries concerning this communication or earlier communications from the examiner should be directed to Tony Mahmoudi whose telephone number is (703) 305-4887. The examiner can normally be reached on Mondays-Fridays from 08:00 am to 04:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached at (703) 305-3830.

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August 27, 2003

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